

The circuit diagram shows a current mirror circuit 200. It includes a PMOS network at the top connected to Vcc (200a) and an NMOS network at the bottom connected to gnd (200b). The PMOS network consists of three parallel branches: a first branch with PMOS transistor M1 (gate N, source 211, drain 205b), a second branch with PMOS transistors M2 and M3 in series (gates 212 and 213, sources 205a and 206a, drains 205 and 206b), and a third branch with a load resistor 231 (drain 205, source 206b). The NMOS network consists of two parallel branches: one with NMOS transistor Q1 (gate 201, source 206a, drain 221) and another with NMOS transistor M (gate 202, source 206b, drain 205b). An input current source I_in (221) is connected between node 221 and gnd. A reference current N*I_in flows through Q1. The output current N*M*I_in flows through the load resistor 231.

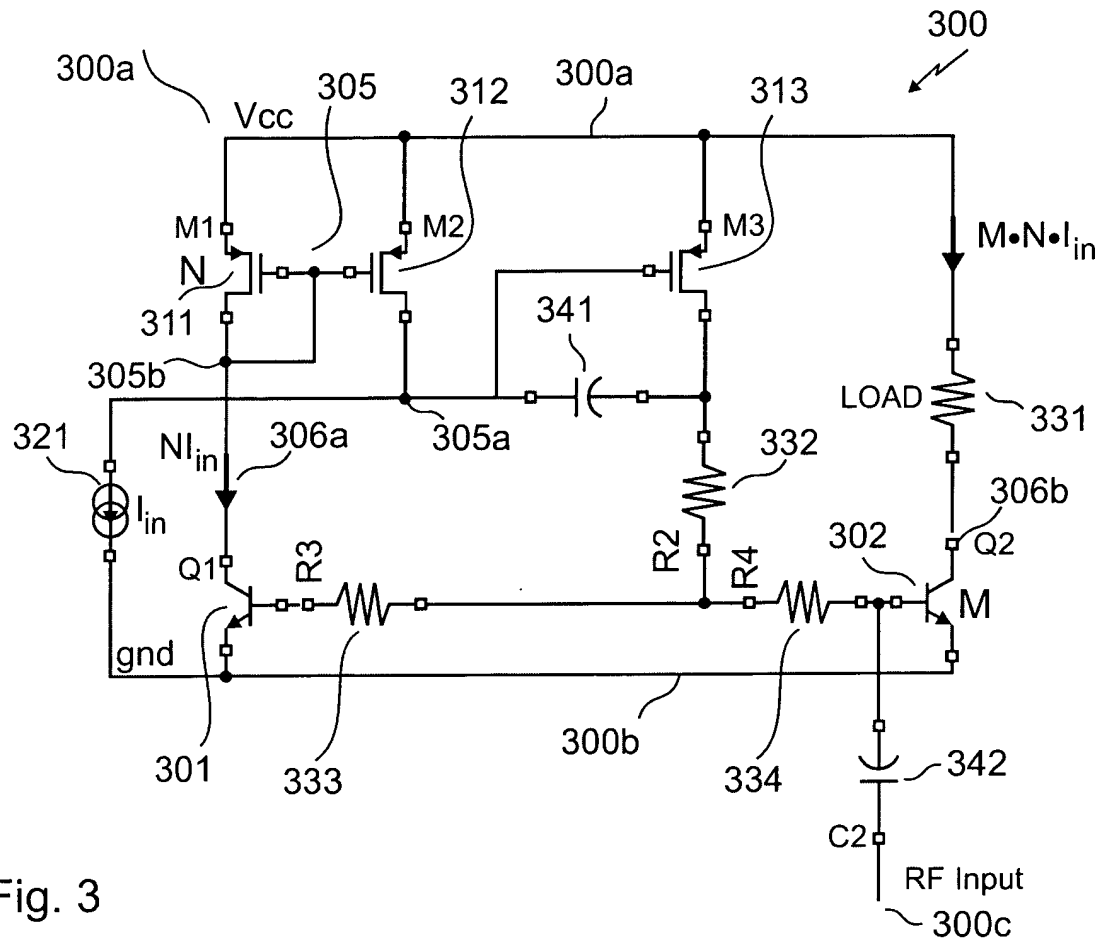


Fig. 3